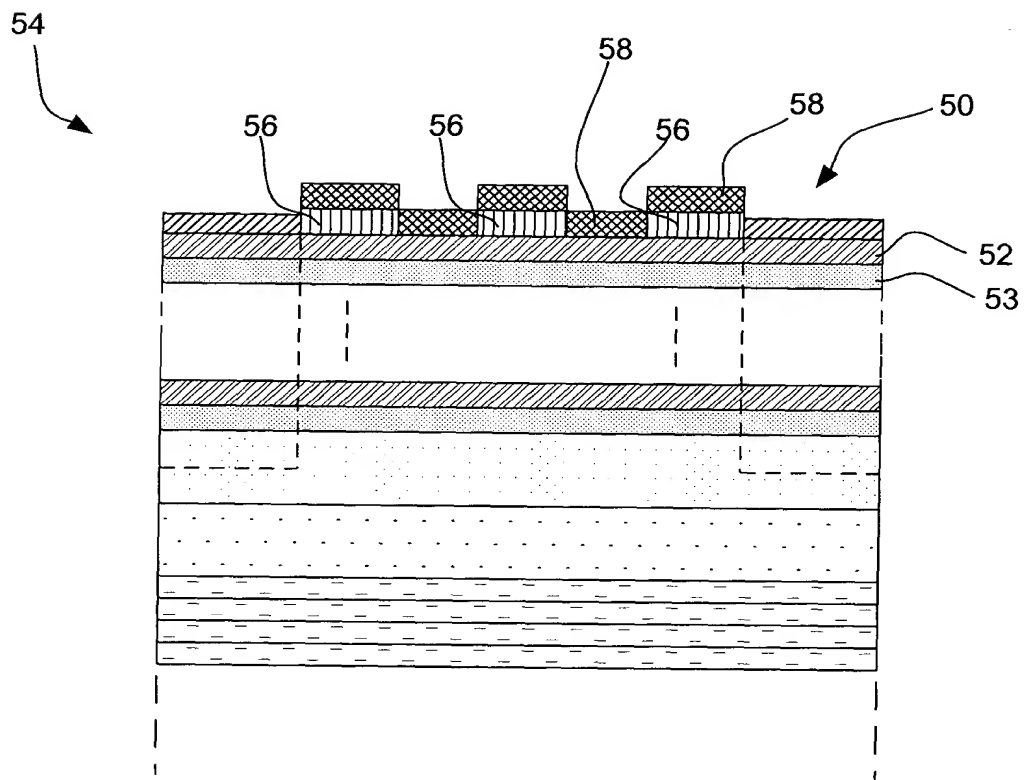
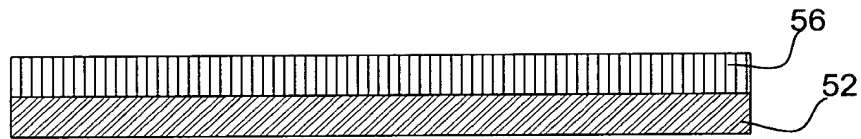


**FIG. 1**

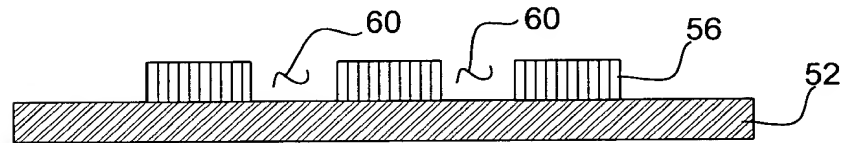
FIG. 2 is a cross-sectional view of a semiconductor device 50, showing a substrate 52 with a top layer 53. A patterned layer 54 is formed on the top layer 53, and a patterned layer 56 is formed on the patterned layer 54. The patterned layer 56 is formed in a series of rectangular blocks 58.



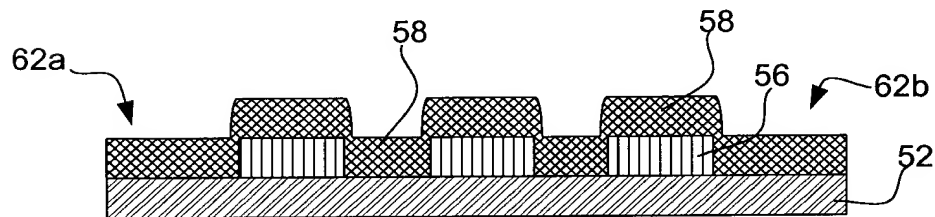
**FIG. 2**



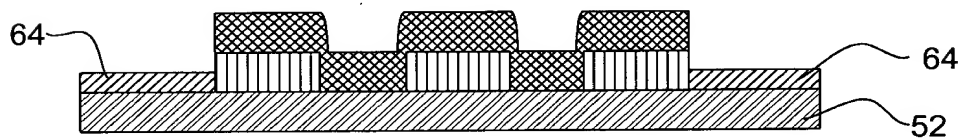
**FIG. 3A**



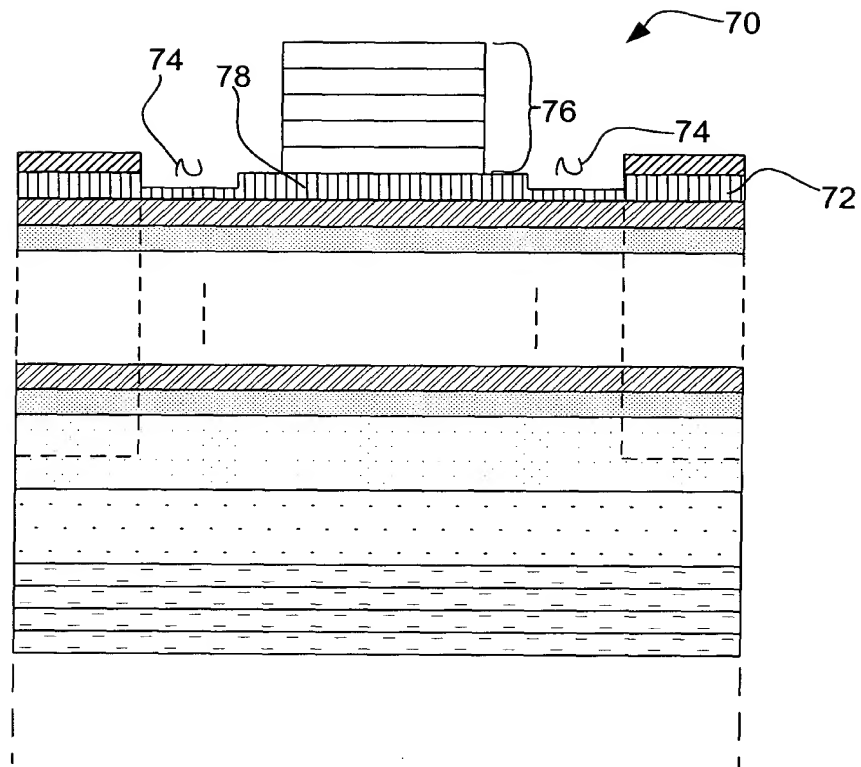
**FIG. 3B**



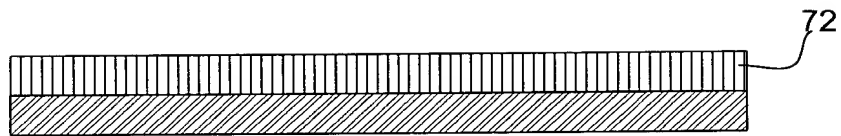
**FIG. 3C**



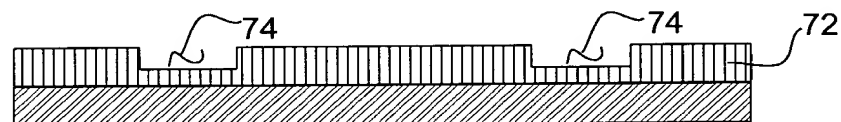
**FIG. 3D**



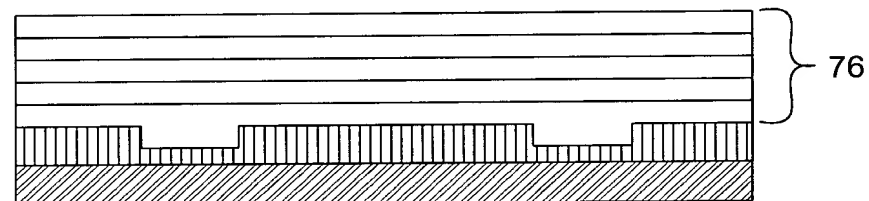
**FIG. 4**



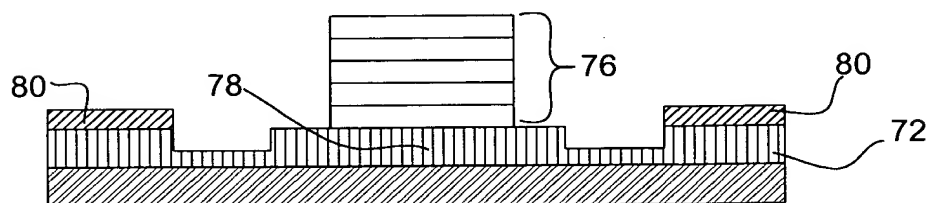
**FIG. 5A**



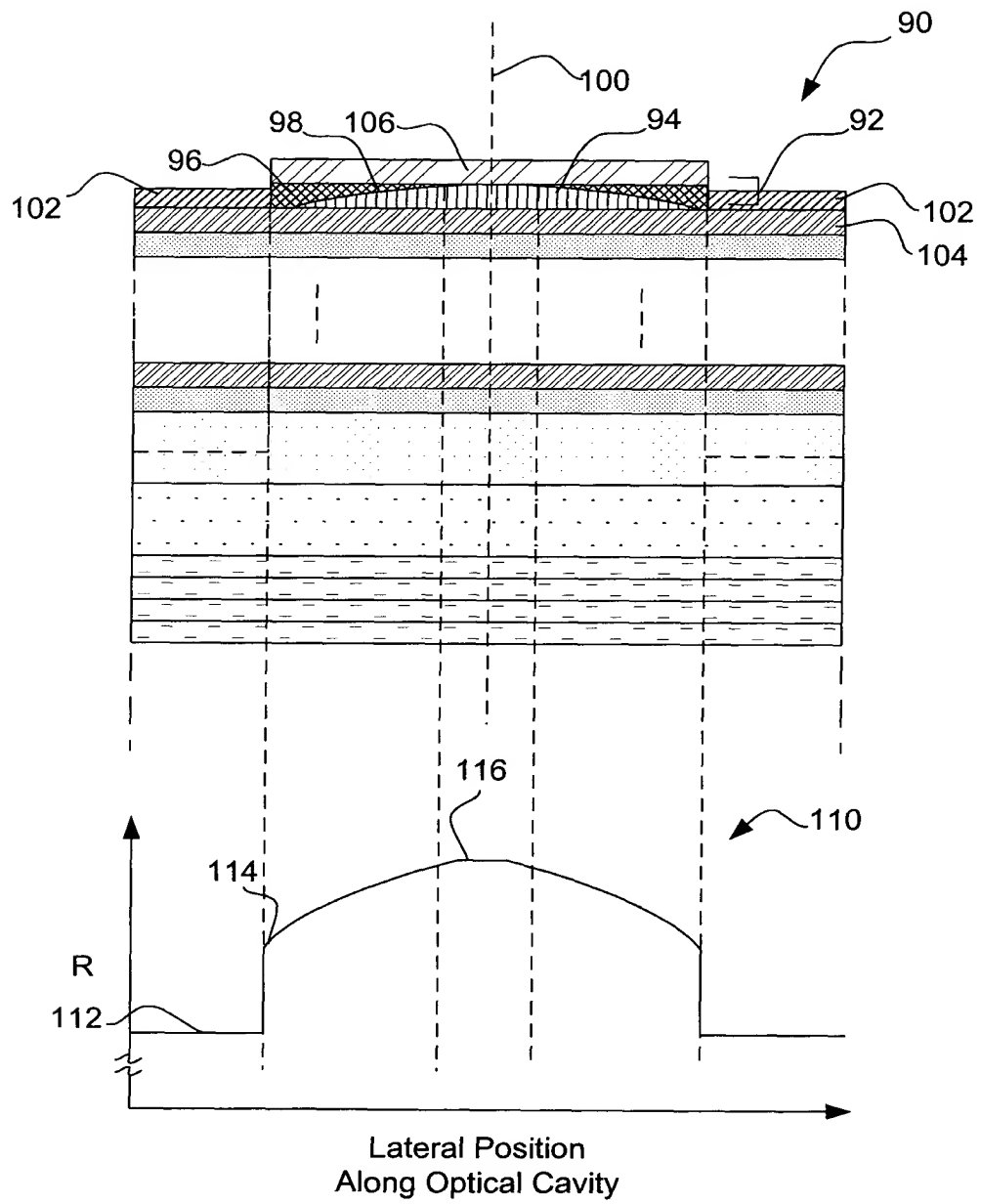
**FIG. 5B**



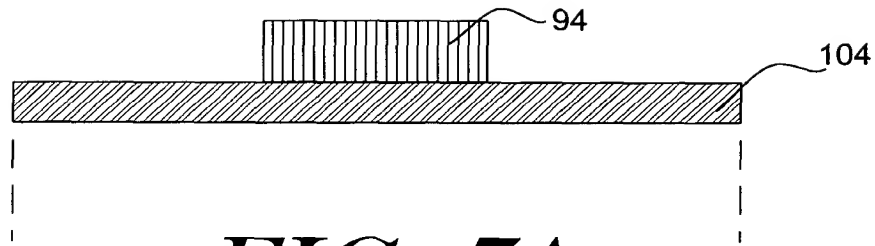
**FIG. 5C**



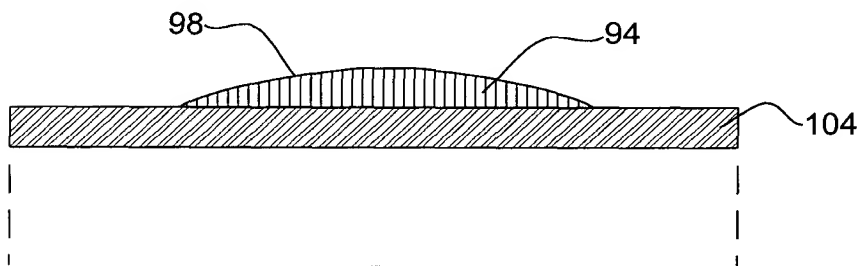
**FIG. 5D**



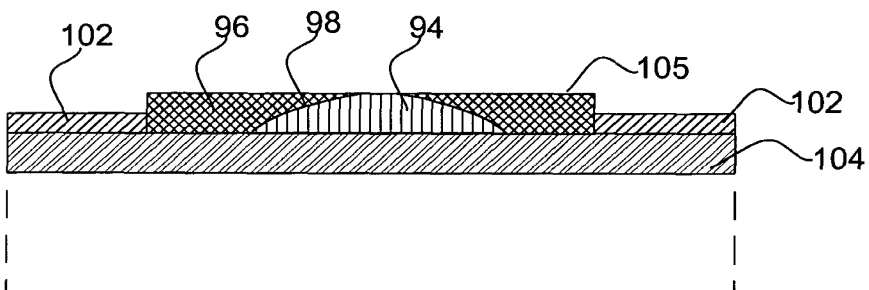
**FIG. 6**



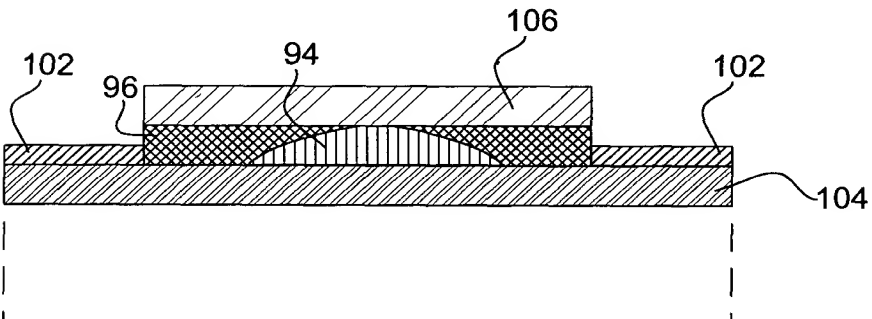
**FIG. 7A**



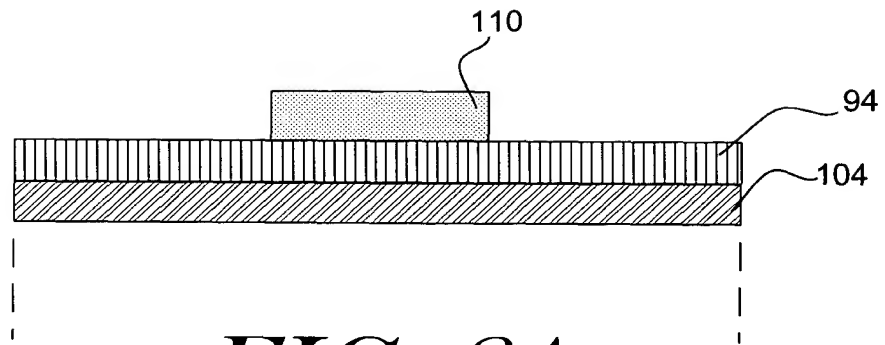
**FIG. 7B**



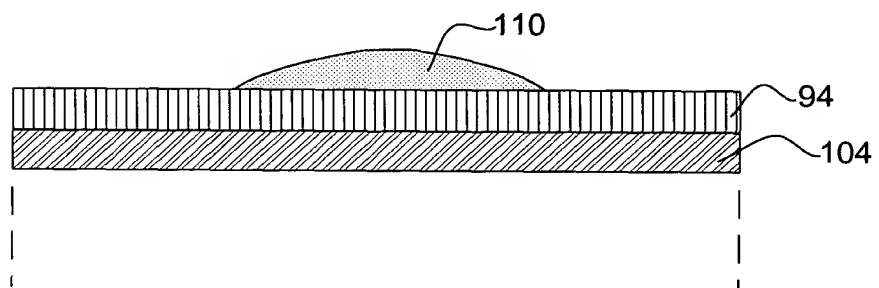
**FIG. 7C**



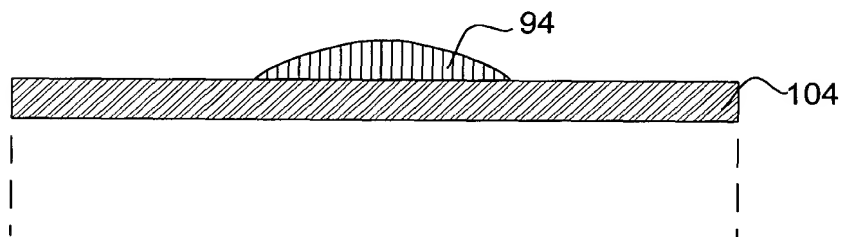
**FIG. 7D**



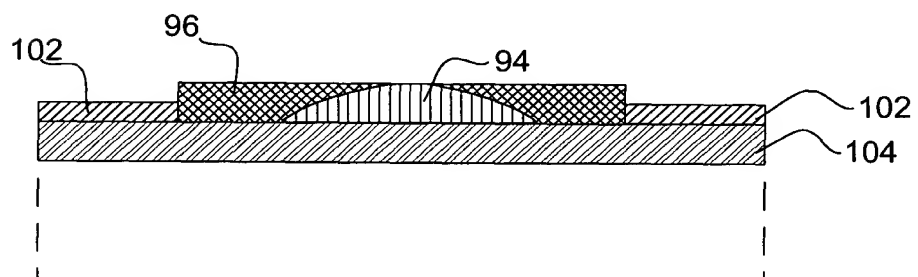
**FIG. 8A**



**FIG. 8B**

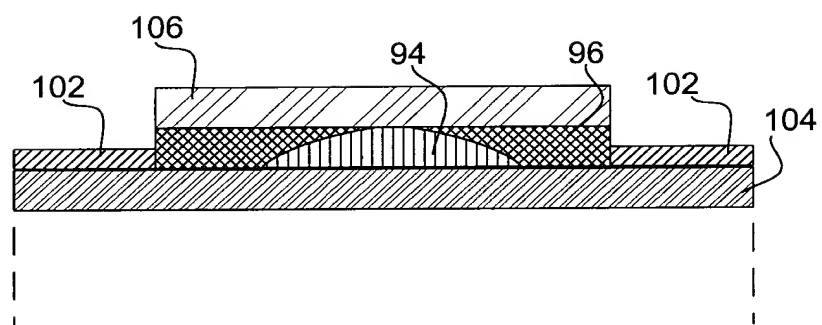


**FIG. 8C**

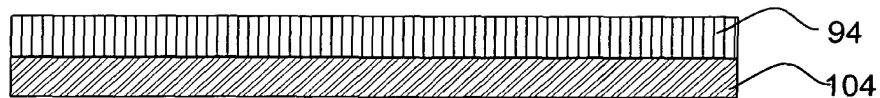


**FIG. 8D**

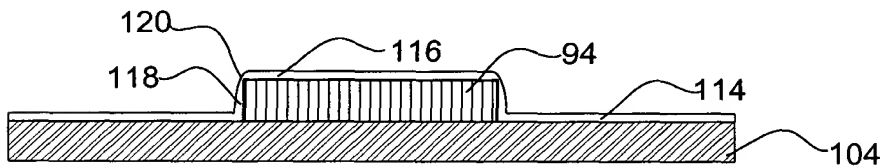




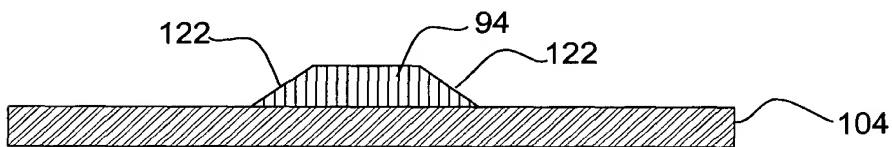
*FIG. 8E*



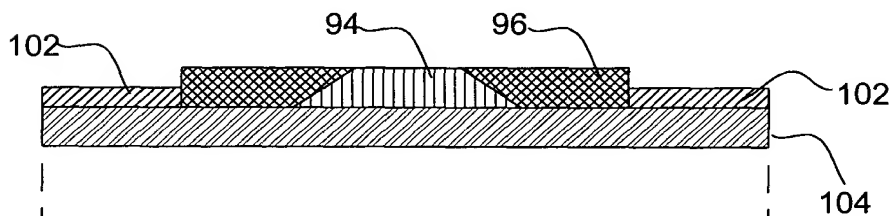
**FIG. 9A**



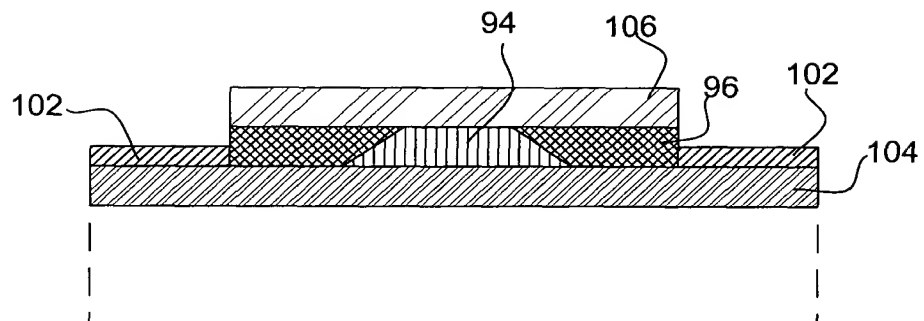
**FIG. 9B**



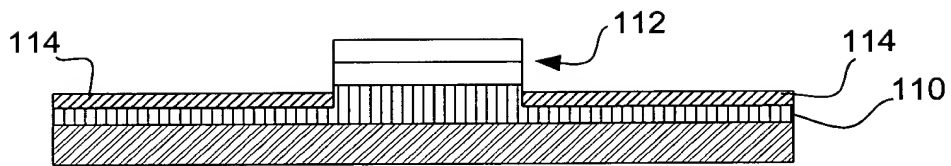
**FIG. 9C**



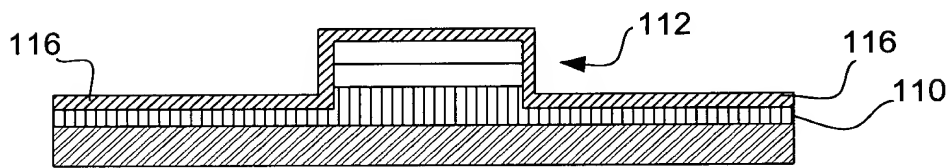
**FIG. 9D**



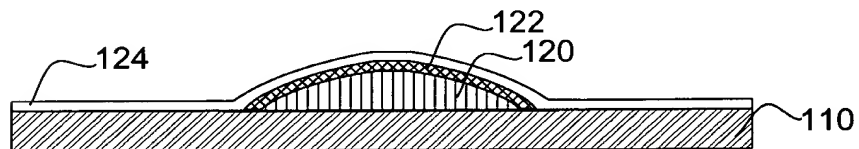
***FIG. 9E***



**FIG. 10**



**FIG. 11**



**FIG. 12**